CLAIMS

1. A method for prioritizing requests in a data processor having a bus interface unit, adapted to be coupled to a communications bus, which services requests for use of the communications bus, and a plurality of resources that make requests for use of the communications bus, a method comprising:

receiving a first request from a first resource and a second request from a second resource;

using a threshold corresponding to one of the first resource and the second resource to assign a priority to the first request.

2. The method of claim 1, wherein using the threshold comprises using status information corresponding to the first and second resource.

3. The method of claim 2, wherein the status information is stored in a static control register.

4. The method of claim 1, wherein the threshold is programmable.

5. The method of claim 4, wherein the threshold is user programmable.

6. The method of claim 4, wherein threshold is capable of being modified during operation of the data processor.

7. The method of claim 6, wherein the threshold is adaptively modified by a performance monitor, in response to evaluating performance of the data processor.

8. The method of claim 1, wherein the first resource comprises a write buffer which makes requests for use of the communications bus for transferring information to a memory.

9. The method of claim 8, wherein the second resource comprises an instruction prefetch buffer which makes requests for use of the communications bus for receiving instructions from the memory.

10. The method of claim 8, wherein the data processor has a cache, adapted to be coupled to the communications bus, and the second resource includes a push buffer which make requests for use of the communications bus for transferring information to the memory.

11. The method of claim 1, wherein the first resource includes an instruction prefetch buffer and the second resource includes a push buffer.

12. A data processor comprising:

a central processing unit;

a first requesting resource coupled to the central processing unit, and adapted to request use of a communications bus for transmitting or receiving data;

a second requesting resource coupled to the central processing unit, and adapted to request use of the communications bus for transmitting or receiving data; and

a bus interface unit coupled to the central processing unit, the first requesting resource, and the second requesting resource, and adapted to be coupled to the communications bus, the bus interface unit further comprising:

a priority controller coupled to receive a first request from the first requesting resource and a second request from the second requesting resource, and to assign a priority to each of the first and second request based on a threshold corresponding to one of the first requesting resource and the second requesting resource.

13. The data processor of claim 12, wherein the priority controller comprises storage circuitry for storing a first resource threshold corresponding to the first requesting resource, a second resource threshold corresponding to the second requesting resource, and a control value corresponding to the first and second requesting resources.

14. The data processor of claim 13, wherein if a number of valid entries of the first requesting resource exceeds the first resource threshold and a number of valid entries of the second requesting resource exceeds the second resource threshold, the priority controller uses the control value to assign the priority to each of the first and second request.

15. The data processor of claim 13, wherein the storage circuitry comprises user programmable registers.

16. The data processor of claim 13, wherein the first resource threshold indicates a first level of the first requesting resource at which priority of the first request should be modified, and the second resource threshold indicates a second level of the second requesting resource at which priority of the second request should be modified.

17. The data processor of claim 13, wherein the priority controller further comprises comparing circuitry coupled to the storage circuitry.

18. The data processor of claim 12, wherein the priority controller comprises priority rules specification circuitry which includes at least one threshold registers for storing the threshold.

19. The data processor of claim 12, where the priority controller further comprises a priority effectiveness monitor coupled to evaluate and selectively modify performance of the priority controller.

20. The data processor of claim 19, wherein selectively modifying performance of the priority controller comprises selectively modifying the threshold.

21. A processor, comprising:

a processing unit;

a cache coupled to the processing unit;

a write buffer coupled to the processing unit;

a priority controller, coupled to the processing unit, the cache, and the write buffer, the priority controller comprising:

priority rules specification circuitry, wherein the priority rules specification circuitry comprises a first programmable threshold register which stores a first threshold corresponding to the write buffer; and

current priority resolution circuitry coupled to the priority rules specification circuitry which receives memory access requests from the cache and the write buffer and which prioritizes the memory access requests based at least on the first threshold.

22. The processor of claim 21, wherein the memory access requests are communicated via a same communications bus.

23. The processor of claim 21, wherein the cache comprises at least one of a data cache or an instruction cache.

24. The processor of claim 21, wherein the first programmable threshold register is capable of being reprogrammed during operation of the processor.

25. The processor of claim 24, wherein the priority controller further comprises a priority effectiveness monitor coupled to the priority rules specification circuitry which monitors operation of the processor.

26. The processor of claim 25, wherein the priority effectiveness monitor selectively reprograms the first programmable threshold register during operation of the processor.

27. The processor of claim 21, further comprising a push buffer coupled to the cache, wherein the priority rules specification circuitry comprises a second programmable threshold register which stores a second threshold corresponding to the push buffer.

28. The processor of claim 27, wherein the current priority resolution circuitry receives memory access requests from the push buffer and prioritizes the memory access requests from the cache, write buffer, and push buffer based one at least one of the first threshold and the second threshold.

29. The processor of claim 21, wherein the priority rules specification circuitry comprises a subthreshold register which stores a subthreshold corresponding to the write buffer.

30. The processor of claim 29, wherein the subthreshold register is user programmable.

31. The processor of claim 29, wherein the current priority resolution circuitry prioritizes the memory access requests based on the subthreshold.

32. A method for prioritizing requests in a data processor having a processing unit, a cache coupled to the processing unit, a write buffer coupled to the processing unit, and a bus interface unit coupled to the processing unit, the cache, and the write buffer, the bus interface unit adapted to be coupled to a communications bus and to service requests from the cache and the write buffer for use of the communications bus, a method comprising:

receiving a first communications bus access request from the cache and a second communications bus access request from the write buffer; and

using a first threshold corresponding to the write buffer to determine which one of the first and second communications bus access requests gets priority.

33. The method of claim 32, further comprising:

modifying the first threshold.

34. The method of claim 32, further comprising:

monitoring operation of the data processor; and

in response to monitoring, selectively modifying the first threshold.

35. The method of claim 32, wherein the bus interface unit includes a control register, and wherein using the first threshold to determine which one of the first and second communications bus access requests gets priority comprises using the control register in addition to the first threshold to determine which one of the first and second communications bus access requests gets priority.

36. The method of claim 32, wherein the data processor comprises a push buffer coupled to the cache and to the bus interface unit, the bus interface unit adapted to service requests from the push buffer for use of the communications bus, the method for prioritizing requests further comprising:

receiving a third communications bus access request from the push buffer; and

using a second threshold corresponding to the push buffer and the first threshold to determine which one of the first, second, and third communications bus access requests get priority.

37. A data processor, comprising:

a processing unit;

a cache coupled to the processing unit;

a write buffer coupled to the processing unit;

a bus interface unit coupled to the processing unit, the cache, and the write buffer, the bus interface unit adapted to be coupled to a communications bus, and which services requests from the cache and the write buffer for use of the communications bus;

receiving means, coupled to the cache and the write buffer, for receiving a first communications bus access request from the cache and a second communications bus access request from the write buffer; and

priority assigning means, coupled to the receiving means, for using a first threshold corresponding to the write buffer to determine which one

of the first and second communications bus access requests gets priority.

38. The data processor of claim 37, further comprising modifying means for selectively modifying the first threshold.

39. In a data processor having a processing unit, a write buffer coupled to the processing unit, and a bus interface unit coupled to the processing unit, the cache, and the write buffer, wherein the bus interface unit is adapted to be coupled to a communications bus and service requests from the write buffer, and the processing unit for use of the communications bus, a method comprising:

receiving an instruction prefetch request corresponding to an instruction prefetch buffer;

comparing a number of valid entries within the write buffer with a write buffer threshold to obtain a first comparison result;

comparing a number of valid entries within the instruction prefetch buffer with an instruction prefetch buffer threshold to obtain a second comparison result; and

assigning a priority to the instruction prefetch request based on the first and second comparison results.

40. The method of claim 39, further comprising:

receiving a second instruction prefetch request; and

modifying at least one of the write buffer threshold and the instruction prefetch buffer threshold prior to receiving the second instruction prefetch request.

41. The method of claim 40, wherein the second instruction prefetch request requests an instruction sequential to an instruction requested by the instruction prefetch request.

42. The method of claim 39, wherein assigning the priority is selectively based further on a static control value.

43. The method of claim 42, wherein if the number of valid entries within the write buffer exceeds the write buffer threshold and the number of valid entries within the instruction prefetch buffer is below the instruction prefetch buffer threshold, assigning the priority is based further on the static control value.

44. The method of claim 39, wherein the data processor further comprises a cache coupled to the processing unit and the write buffer, wherein the write buffer comprises a push buffer.

45. The method of claim 39, further comprising:

receiving a data request; and

assigning a priority to the data request based on the first and second comparison results.

46. The method of claim 39, wherein assigning the priority is further based on a subthreshold value corresponding to at least one of the write buffer and the instruction prefetch buffer.

47. A data processor, comprising:

processing unit;

a write buffer coupled to the processing unit; and

a bus interface unit coupled to the processing unit and the write buffer, wherein the bus interface unit is adapted to be coupled to a communications bus and service requests from the write buffer, and the processing unit for use of the communications bus, the bus interface unit comprising:

receiving means for receiving an instruction prefetch request corresponding to an instruction prefetch buffer;

first comparing means, coupled to the receiving means, for comparing a number of valid entries within the write buffer with a write buffer threshold to obtain a first comparison result;

second comparing means, coupled to the receiving means, for comparing a number of valid entries within the instruction prefetch buffer with an instruction prefetch buffer threshold to obtain a second comparison result; and

priority means, coupled to the first and second comparing means, for assigning a priority to the instruction prefetch request based on the first and second comparison results.

48. The data processor of claim 47, further comprising modifying means for modifying at least one of the write buffer threshold and the instruction prefetch buffer threshold prior to receiving a second instruction prefetch request.

49. The data processor of claim 47, wherein the priority means assigns the priority based further on a subthreshold value corresponding to at least one of the write buffer and the instruction prefetch buffer.

50. In a data processor having a processing unit, a write buffer having a plurality of entries and coupled to the processing unit, and a bus interface unit coupled to the processing unit and the write buffer, the bus interface unit adapted to be coupled to a communications bus and service requests from the write buffer and the processing unit for use of the communications bus, a method comprising:

receiving a read request;

upon receiving the read request, detecting a write buffer collision at a colliding entry in the write buffer; and

in response to detecting the write buffer collision, flushing a portion of the plurality of entries in the write buffer, including the colliding entry.

51. The method of claim 50, wherein the portion of the plurality of entries in the write buffer includes all entries prior to the colliding entry.

52. The method of claim 50, wherein detecting the write buffer collision comprises comparing address bits of valid entries in write buffer with address bits of the read request.

53. A data processor comprising:

a processing unit;

a write buffer having a plurality of entries and coupled to the processing unit;

a bus interface unit coupled to the processing unit and the write buffer, the bus interface unit adapted to be coupled to a communications bus and service requests from the write buffer and the processing unit for use of the communications bus;

receiving means coupled to the bus interface unit for receiving a read request;

detecting means coupled to the receiving means for detecting a write buffer collision at a colliding entry in the write buffer upon receiving the read request; and

flushing means coupled to the detecting means for flushing a portion of the plurality of entries in the write buffer, including the colliding entry, in response to detecting the write buffer collision.

54. In a data processor having a processing unit, the processing unit having a prefetch buffer, and a bus interface unit coupled to the processing unit, the bus interface unit adapted to be coupled to a communications bus and service requests from the prefetch buffer and the processing unit for use of the communications bus, a method comprising:

receiving a change of flow instruction fetch request;

comparing a number of entries within the prefetch buffer with a prefetch buffer threshold; and

in response to comparing the number of entries, selectively affecting a priority of the change of flow instruction fetch request with respect to a request from the prefetch buffer for use of the communications bus.

55. The method of claim 54, wherein selectively affecting the priority of the change of flow instruction fetch request is based on a static control value corresponding to a priority policy for change of flow instructions.

56. A method for prioritizing requests in a data processor having a bus interface unit, adapted to be coupled to a communications bus and which services requests for use of the communications bus, a first requesting resource, and a second requesting resource, wherein the first and second requesting resources make requests for use of the communications bus, a method comprising:

selectively receiving a first request from a first resource and selectively receiving a second request from a second resource;

if the first request and the second request are received, using a threshold corresponding to one of the first resource and the second resource to assign priorities to the first and second request; and

if the first request and the second request are not received:

comparing a number of entries within the first requesting resource to a first requesting resource threshold and comparing a

number of entries within the second requesting resource to a second requesting resource threshold; and

if the number of entries within the first requesting resource falls below the first requesting resource threshold and the number of entries within the second requesting resource falls below the second requesting resource threshold, using a subthreshold corresponding to one of the first requesting resource and the second requesting resource to assign priorities to the first and second request.

57. The method of claim 56, wherein the first resource is one of a write buffer, a prefetch buffer, and a push buffer, and the second resource is one of a write buffer, a prefetch buffer, and a push buffer.